AVR2005: Design Considerations for the AT86RF230

Application Note

Features

- **General considerations**
- **Power supply**
- **Harmonic suppression**
- **System reactions to foreign signals**

1 Introduction

The ATAVRRZ502 is designed for evaluation of the Atmel AT86RF230 2.4 GHz radio transceiver. This radio transceiver fully complies with the IEEE 802.15.4™ standard and targets low-power wireless technologies within home, building and industrial automation application, such as ZigBee™.

This application note describes the design and layout of the so-called "Radio Extender Board" (REB) that are provided with the ATAVRRZ502. The information provided is intended as a helping hand for hardware designers implementing a design using the AT86RF230.

The REB can be seen in Figure 1-1.

Figure 1-1. ATAVRRZ502 Accessory Kit's Radio Extender Board.

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2 Layout description

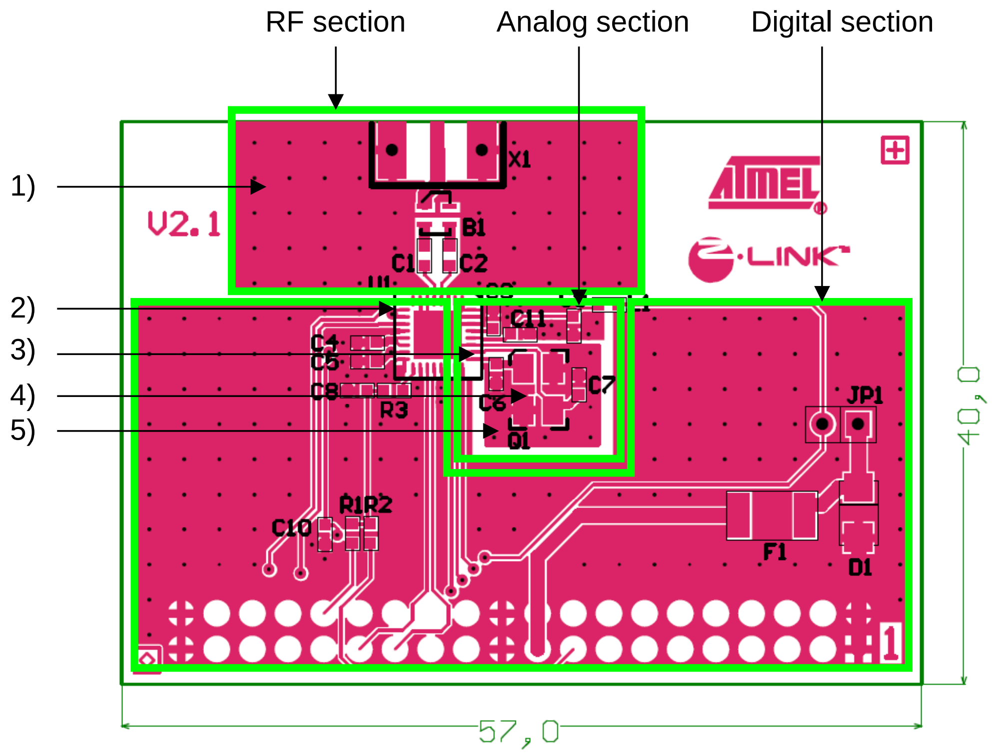
This section provides an introduction as to how the layout around the AT86RF230 should be segmented. It will point out the critical areas around the AT86RF230 and recommends proper layout exemplary done on a Radio Extender Board.

2.1 General

The layout around the AT86RF230 can be viewed as being divided into digital, analog and RF layout domains/areas. Digital layout area contains signals such as Reset, interrupt request lines (IRQ) and SPI interface lines. Power supply and the crystal is contained within the analog layout area. The RF layout area includes the antenna signals, supply decoupling, and the geometry of the ground planes around the IC. The sensitive areas are:

- Areas of the AT86RF230 running at 16MHz.
- The CLKM pin (radio main clock) driving a continuous clock output signal.
- Digital outputs, such are SPI communications and clock lines.

Figure 2-1. ATAVRRZ502 Accessory Kit's Radio Extender Board Layout.



1. Antenna ground plane.
2. AT86RF230 radio (U1 in schematic/ silkscreen).
3. Signals U1.XTAL1 and U1.XTAL2.
4. 16MHz crystal.
5. Crystal ground plane.

The routing of the RF output pins RFP (positive output to antenna) and RFN (negative output to antenna) of the AT86RF230, which must connected via a series capacitor to the balun input, must be impedance controlled lines of 100 ohms (differential impedance). This is required to get best RF performance.

In the same manner the connection from the balun output to the SMA connector must be designed to have 50 ohms impedance. The capacitors in the RF path (C1 and C2 in Figure 2-1/Figure 3-1) shall be no larger that 0603 in size, and of NP0 or C0G type. The trace from the IC pins to the capacitors should have an impedance in the range of 1 to 2 nH.

All trace from the radio to balun, and from the balun to the antenna must be designed symmetrically to ensure that the two traces have same impedance.

Trace and planes used for power and ground routing should be wide and as coherent as possible to provide lowest impedance possible. Multiple via connections shall be placed between the layers if multiple grounding layers are used to minimize the impedance.

The isolation between two neighboring pins one the RF230 should be larger than 10 Mohm when the board is cleaned in the manufacturing process. Be aware that residuals from the soldering can potentially affect the isolation between the pins.

2.2 Power supply and ground areas

Since noise is in evidently present on power and ground signals, as well as on other signal lines, there is no perfect way of shortening or filtering traces to eliminate it. As shown in Figure 2-1, the circuitry necessary for using the AT86RF230 is separated into three separate ground planes therefore. This is done to minimize the noise contamination from one ground area to the other. The 16MHz crystal, antenna, analog, digital and power supply sections are divided to isolate the special IC blocks as well as possible. The ground pad of the AT86RF230 (bottom side) shall act as the star point of the ground areas, so all ground areas are connected here as the only common point.

The antenna is separated from the rest of the design so that it does not induce modulation of the analog ground either via the crystal or power supply and as a consequence create self-modulation effects. These effects could cause problems meeting FCC or ETSI government regulations.

The power supply decoupling is according to the description in the AT86RF230's datasheet (section 10.2), which means standard 1uF capacitors on each of the supply pins AVDD, DVDD, and DEVDD.

To avoid injecting noise from one ground signal to another, all ground signals should be connected at one placed on the board in a star topology. It is recommended to set this connection point right on the AT86RF230 pad (bottom plate) for providing the shortest resistance to the IC's transceiver blocks for minimum noise levels.

2.3 Crystal and harmonic suppression

The 16MHz crystal and its capacitors are kept on a separate ground plane to reduce the RF power on the antenna ground. This ground plane is connected to the IC's ground signal by a minimal trace (0.15 to 0.2 mm wide) close to C11 in Figure 2-2 (see schematic in Figure 3-1) to provide low non-zero impedance to the main ground. This route should not be longer then 6mm to not get too high resistance. It is recommended to surround the crystal ground plane by a ground free area that is approximately 1mm wide on the top and bottom sides.

Additionally all digital signals, such as the SPI clock, should be shielded from the crystal ground area to suppress crosstalk by using a ground signal trace (digital ground) in between the digital trace and the ground free space around the crystal. This will suppress crosstalk which can produce receive errors. All signals should have a parallel ground trace in very close proximity, or alternatively be “covered” by a ground plane on the back-side of the PCB. The ground used in this case must be digital or analog ground, NOT RF ground. If RF ground are used this will inject transient into the RF ground and affect the RF performance.

Figure 2-2. Crystal layout part, top layer.

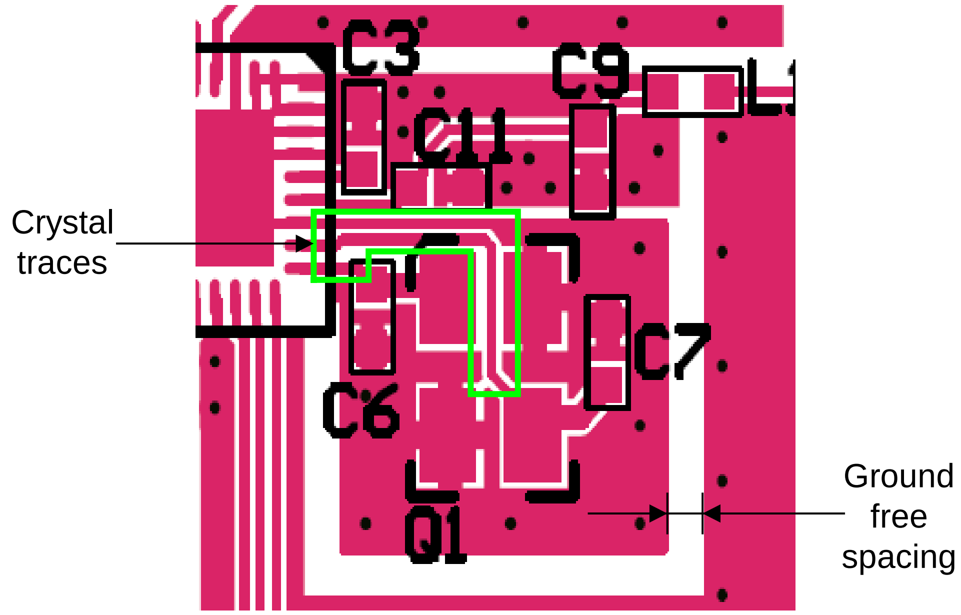
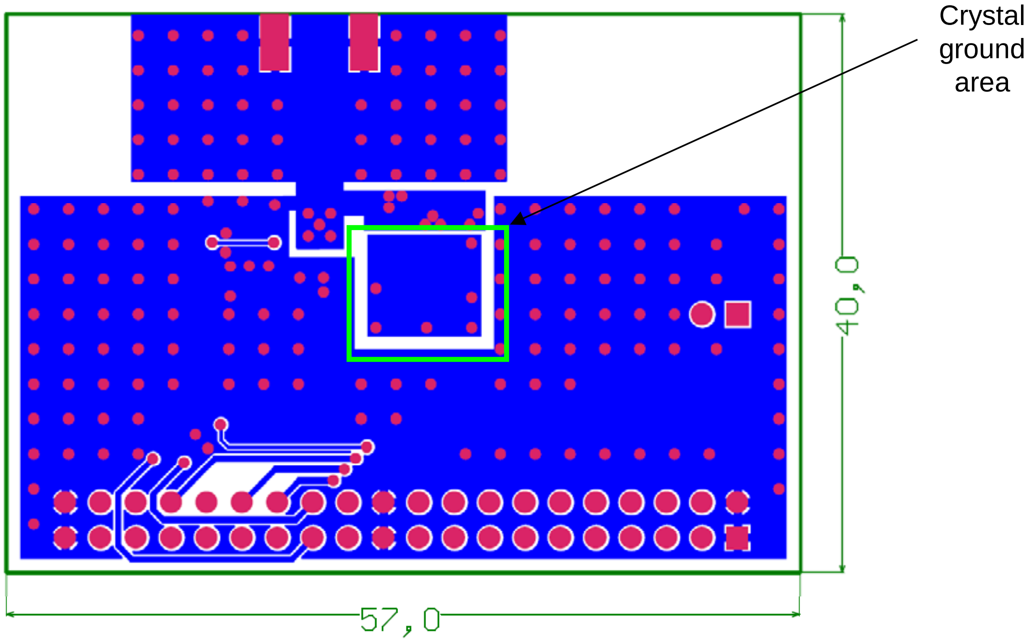


Figure 2-3. Crystal layout part, bottom layer.



2.4 Clock driver CLKM

CLKM pin (RF230 main clock output) can be used to clock other parts of the design, e.g. the microcontroller: Since the signal provided by the CLKM pin has fast rail-to-rail transitions, filtering is required. Otherwise spurious emissions may be seen in the RF domain in the transmitted signal. The following two criteria exist for this filter:

- Frequencies above (100 +/- 20) MHz should be attenuated by at least 3dB
- CLKM pin can drive VDD with 2mA current

A 1st order low pass filter will be fine to archive the values given in table 2-1. The combination of a resistor and capacitor as shown in Figure 2-4 is recommended to provide the desired functionality and fulfils the filter function. The trace used to connect the filter between the AT86RF230 CLKM pin and the destination must have a width allowing an impulse of 6ns (capacitive load), if the CLKM signal is used as a 16MHz clock source.

Figure 2-4. CLKM low pass filter.

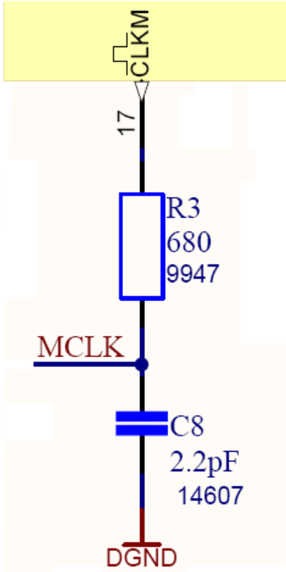
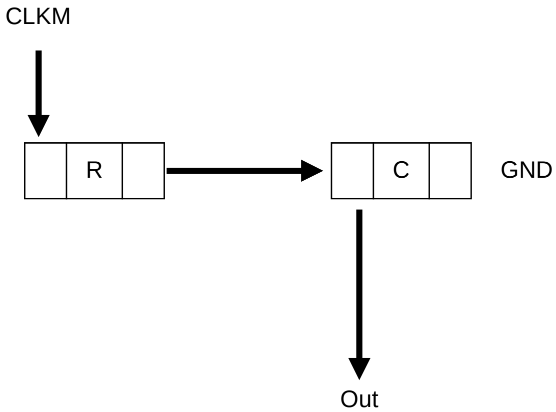


Table 2-1. Special points of filter function.

Frequency	Attenuation [dB]
130 MHz	~ 3
1.2 GHz	~ 20

Figure 2-5. CLKM filter placing.



Make sure that the filter output signal comes directly from the capacitor component (as shown in Figure 2-5) to insure that the board impedance is used correctly.

2.5 Undesired System Reaction

The receiving process consists of an endless loop of signal acquisition and reception. During the acquisition stage the RF level at the antenna input is checked to be the preamble phase of the signal. This is done by autocorrelating the input signal and the spreading sequence. Here every input (whether it is noise or a sinusoidal signal) is expected to be a potential spreaded signal until the correct synchronization word is detected. Therefore it is it should be expected that a continuous wave (CW) carrier might start the autocorrelation process and a reception.

This means that if a CW carrier or high noise is present, it is likely that the real frame, which is now masked, can not be received since the receiver is blocked due to accidentally detection of a frame in the noise floor, or the endlessly unsuccessful correlation of the CW carrier searching for the synchronization word.

Self-produced CW carriers and board noise are the closest interfering signals, since their source is located on the same board as the receiver. Due to system design the most affected channels are shown in table 2-2. The system uses a 16MHz crystal to operate. This 16MHz oscillator produces more or less harmonics depending on the layout around the crystal. E.g.: the 155th harmonic of the 16MHz crystal will produce a CW carrier of about -100 dBm at 2.48GHz, which is channel 26. Usually this is at the border level, in this case is about -101dBm, but this can increase up to -80dBm with improper layout. These signal levels are definitely large enough to be despreaded and handed over to the next higher layer with a bad CRC, a random length and containing random data. Avoid additional CW carrier generation caused by an improper layout.

Table 2-2. Self-interferes frequencies.

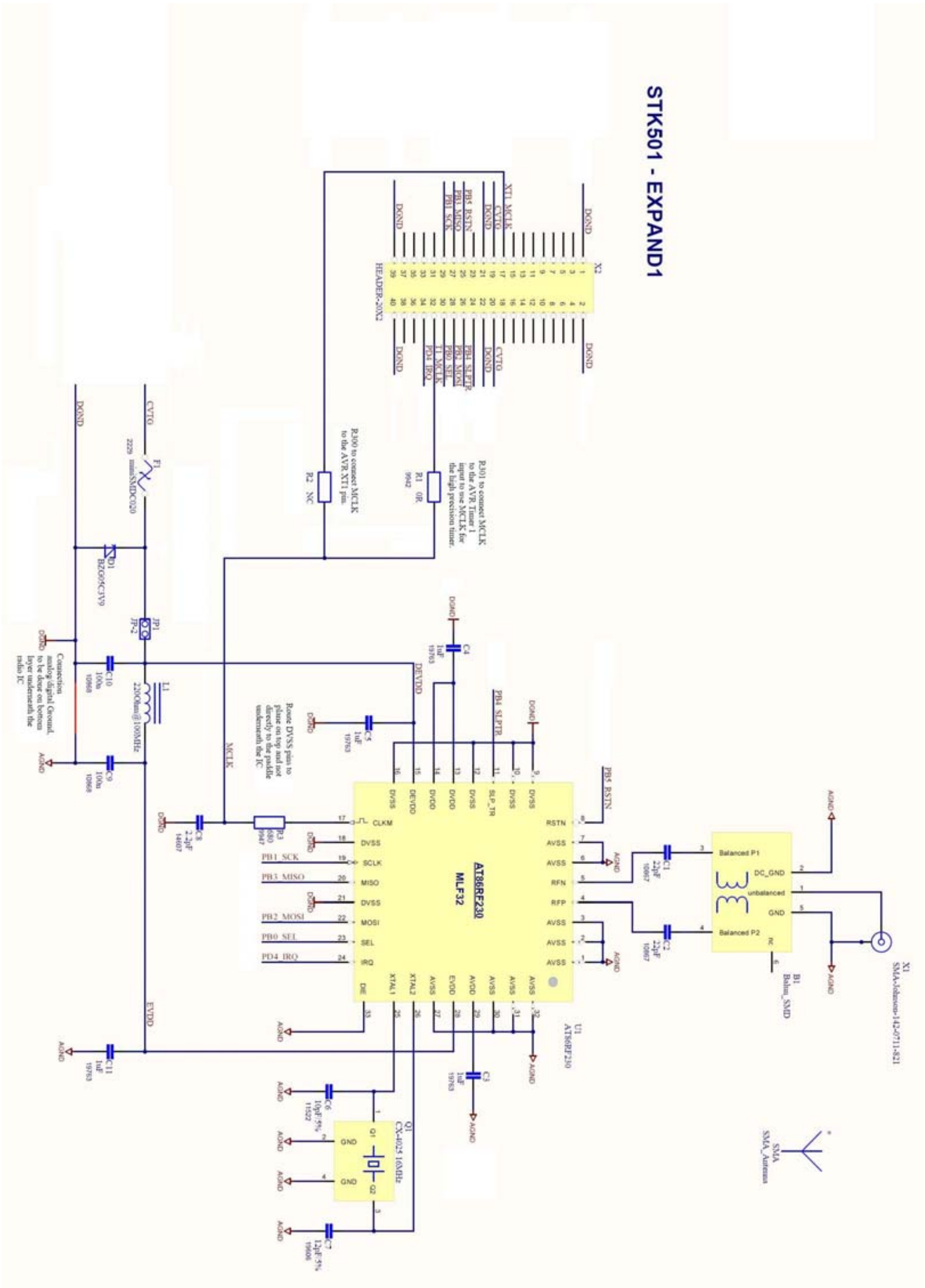
Channel	Frequency [MHz]	Self-made interferes frequency [MHz]
13	2415	2416
23	2465	2464
26	2480	2480

2.6 Using external clock

If an external 16MHz clock source is used, the clock must follow the accuracy requirements conform to the IEEE802.15.4™ standard. The IEEE802.15.4™ specifies a timing accuracy for the transmitted signals of +/- 40ppm per symbol or better over the complete product’s operating range. The 16MHz crystal has to provide this accuracy too. In the case the external clock source is able to provide this, the RF frame is still IEEE80215.4™ compliant. Otherwise interoperability with other systems is not given. Even data transmissions between two AT86RF230s will not be possible anymore, when the accuracy is decreased to more than the tolerated +/-60ppm (AT86RF230 datasheet).

3 Schematic of Radio Board

Figure 3-1. Radio Board – Crystal layout part, top layer.



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