TMS320 DSP Algorithm Interoperability Standard

QualiTI Compliance Testing

Compliance Test Report

Date	Thursday, January 16, 2003, 15:29, India Standard Time
Vendor	TI
Algorithm	SRC
Generic Interface	None
Version	3.0
Serial Number	1234
Test Result	**PASS**

Test Notes

This report has been generated with QualiTI Version 2.0.2 Beta - the new XDAIS compliance test suite.

All references to Rules and Guidelines are from the literature numbered SPRU352D, January 2001.

The Rules 17, 18, 25, 26, 27, 28, 29, 30, IDMA 1, IDMA 2, IDMA 3, IDMA 4, IDMA 5 are not applicable and hence were not tested.

If worst case heap memory creation parameter is not provided explicitly then QualiTI tests rule 19 with default instance creation parameter

If you have any questions or comments about the test results below, please send an email message to: algtesters@list.ti.com

Documentation:

D:\pautils\srcc55x_xdais_TI_internal_Api\docs\SRC reference user's guide.doc

Header File(s):

D:\pautils\srcc55x_xdais_TI_internal_Api\algorithm\include\smplrate.h
D:\pautils\srcc55x_xdais_TI_internal_Api\interface\include\src_ti.h
D:\pautils\srcc55x_xdais_TI_internal_Api\interface\include\ialgmods.h
D:\pautils\srcc55x_xdais_TI_internal_Api\interface\include\isrc.h
D:\pautils\srcc55x_xdais_TI_internal_Api\interface\include\ialg.h
D:\pautils\srcc55x_xdais_TI_internal_Api\interface\include\std.h
D:\pautils\srcc55x_xdais_TI_internal_Api\interface\include\xdas.h
D:\pautils\srcc55x_xdais_TI_internal_Api\algorithm\include\src_ti_prvt.h

Algorithm Archive(s):

D:\pautils\srcc55x_xdais_TI_internal_Api\application\build\src_ti.l55

Source File Defining IMOD_PARAMS:
D:\pautils\srcc55x_xdais_TI_internal_Api\interface\src\isrc.c

Source File Defining Worst Case Heap Memory Parametrs:
D:\pautils\srcc55x_xdais_TI_internal_Api\algorithm\src\src_ti_ialg.c

Screening Test: All algorithms must have at least one top level header file named mod_vend.h that includes all the other header file that are provided with the algorithm. In addition the following external symbols MOD_VEND_IALG and MOD_VEND_IMOD / MOD_VEND_IGENERICINTERFACE must be present for the algorithm to be tested.

Report: **Passed**

Details: QualiTI passes this rule after testing

Rule 1: All algorithms must follow the run-time conventions imposed by TI's implementation of the C programming language.

Report: **Passed**

Details: Vendor states compliance in the documentation

Rule 2: All algorithms must be reentrant within a preemptive environment (including time-sliced preemption)

Report: **Passed**

Details: Vendor states compliance in the documentation

Rule 3: All algorithm data references must be fully relocatable (subject to alignment requirements). That is, there must be no "hard coded" data memory locations.

Report: **Passed**

Details: Vendor states compliance in the documentation

Rule 4: All algorithm code must be fully relocatable. That is, there can be no hard coded program memory locations.

Report: **Passed**

Details: Vendor states compliance in the documentation

Rule 5: Algorithms must characterize their ROM-ability; i.e., state whether they are ROM-able or not.

Report: **Passed**

Details: Characterized by the vendor

Rule 6: Algorithms must never directly access any peripheral device. This includes but is not limited to on-

chip DMAs, timers, I/O devices, and cache control registers.

Report: **Passed**

Details: Vendor states compliance in the documentation

Rule 7: All header files must support multiple inclusions within a single source file.

Report: **Passed**

Details: QualiTI passes this rule after testing

Rule 8: All external definitions must be either API identifiers or API and vendor prefixed.

Report: **Passed**

Details: QualiTI passes this rule after testing

Rule 9: All undefined references must refer either to the operations specified in Appendix B (a subset of C runtime support library functions and the DSP/BIOS) or other XDAIS-compliant modules.

Report: **Passed**

Details: QualiTI passes this rule after testing

Rule 10: All modules must follow the naming conventions of the DSP/BIOS for those external declarations disclosed to the client.

Report: **Passed**

Details: Vendor states compliance in the documentation

```
QualiTI has produced a list of exposed external symbols for the user to
verify that DSP/BIOS naming conventions have been followed.

List of exposed external symbols
SRC_TI_exit
SRC_TI_init
SRC_TI_IALG
SRC_TI_ISRC
```

Rule 11: All modules must supply an initialization and finalization method.

Report: **Passed**

Details: QualiTI passes this rule after testing

Rule 12: All algorithms must implement the IALG interface.

Report: Passed

Details: QualiTI passes this rule after testing

Rule 13: Each of the IALG methods implemented by an algorithm must be independently relocatable.

Report: Passed

Details: QualiTI passes this rule after testing

Rule 14: All abstract algorithm interfaces must derive from the IALG interface.

Report: Passed

Details: QualiTI passes this rule after testing

Rule 15: Each XDAIS-compliant algorithm must be packaged in an archive which has a name that follows a uniform naming convention.

Report: Passed

Details: QualiTI passes this rule after testing

Rule 16: Each XDAIS-compliant algorithm header must follow a uniform naming convention.

Report: Passed

Details: QualiTI passes this rule after testing

Rule 19: All algorithms must characterize their worst-case heap data memory requirements (including alignment).

Report: Passed

Details: QualiTI has generated the data

Table of heap memory usage

memTab	Given Attribute	Calculated Attribute	Given Size (bytes)	Calculated Size (bytes)	Given Align	Calculated Align	Given Space	Calculated Space
0	Not Given	PERSISTENT	Not Given	312	Not Given	32	Not Given	IALG_SARAM

Rule 20: All algorithms must characterize their worst-case stack space memory requirements (including alignment).

Report: Passed

Details: Characterized by the vendor

Rule 21: Algorithms must characterize their static data memory requirements.

Report: **Passed**

Details: QualiTI has generated the data

Table of static data memory usage

Section Number	Object File Name	Section Name	Given Size (bytes)	Calculated Size (bytes)	Given Alignment
0	srccoef.obj	.const	Not Given	1808	Not Given
1	src_ti_apply.ob	.const	Not Given	252	Not Given
2	src_ti_rate.obj	.const	Not Given	162	Not Given
3	src_ti_vtable.o	.const	Not Given	80	Not Given
4	smplrate.obj	.const	Not Given	36	Not Given

Rule 22: All algorithms must characterize their program memory requirements.

Report: **Passed**

Details: QualiTI has generated the data

Table of program memory usage

Section Number	Section Name	Given Size (bytes)	Calculated Size (bytes)	Given Alignment
0	.text:algInit	Not Given	317	Not Given
1	.text:algAlloc	Not Given	41	Not Given
2	.text:algFree	Not Given	25	Not Given
3	.text:algNumAlloc	Not Given	4	Not Given
4	.text	Not Given	1682	Not Given
5	.text:exit	Not Given	2	Not Given
6	.text:init	Not Given	2	Not Given

Rule 23: All algorithms must characterize their worst-case interrupt latency for every operation.

Report: **Passed**

Details: Characterized by the vendor

Rule 24: All algorithms must characterize the typical period and worst-case execution time for each operation.

Report: **Passed**

Details: Characterized by the vendor

Rule 31: All C55X algorithms must document the content of the stack configuration register that they follow.

Report: **Passed**

Details: Characterized by the vendor

Rule 32: All C55X algorithms must access all static and global data as far data; also the algorithms should be instantiable in a large memory model.

Report: **Passed**

Details: Vendor states compliance in the documentation

Rule 33: C55X algorithms must never assume placement in on-chip program memory; i.e., they must properly operate with program memory operated in instruction cache mode.

Report: **Passed**

Details: Vendor states compliance in the documentation

Rule 34: C55X algorithms must document the instance number of the IALG_MemRec structure that is accessed by the B-Bus.

Report: **Passed**

Details: Characterized by the vendor