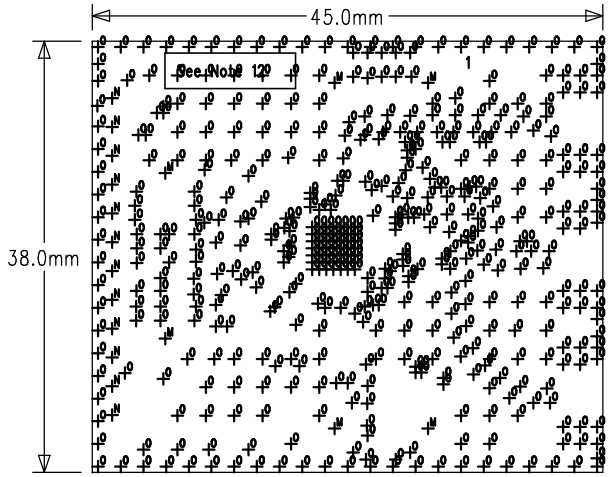


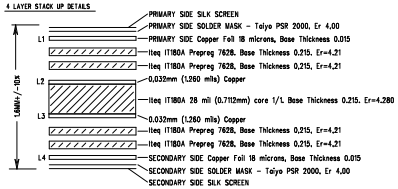
EV-ADF70301-169BZ (08-042809 Rev-A) - Component Side View
Layer 1- Component Side - (Signal & Ground)
Fabrication Drawing

SIZE	QTY	SYM	PLATED	TOL
55	6	M	NO	+/-0.0
39.37	12	N	YES	+/-0.0
7.87	474	O	YES	+/-0.0

MANUFACTURING NOTES

1. Material: 4 Layer, FR4 IT180A glass epoxy laminate, 1.6MM +/- 10% thick.
   Material to be RoHS compliant. Board to be fabricated per IPC-6012A, CLASS 2.
2. Plated thru holes and the conductive pattern electroplated with .0255MM min. thick copper. Terminal areas and plated thru holes to be ENIG plated.
3. Finished Board to be RoHS Compliant
4. Datum for ($x_{,y}$) co-ordinate drill files at Lower Left Fiducial.
5. Processing tolerances:
   A. Conductive pattern front to back registration within .125MM total.
   B. Minimum annular ring surrounding holes: .05MM
   C. Finished conductive pattern within .05MM of true size.
   D. Minimum feature size = 0.2mm.
   E. Minimum air gap = 0.15mm
6. Warp and twist within .1875MM per 25MM (0.75%)
7. Dimensions in mm (millimeters) and are for the finished part.
8. Solder Mask: Taiyo PSR 2000. Liquid photo imagable solder mask over bare copper (smobc), colour GREEN, both sides using the patterns provided. No mask is permitted on the terminal areas. Soldermask to etch registration within .125MM total.
9. Screening: Screen component outlines and nomenclature using indelible white ink on both the primary and secondary side. Nomenclature shall be legible. Screen to etch registration within .15MM total.
10. Boards to be electrically Tested 100%
11. Break all sharp edges 0.35MM R max.
12. Manufacturer to add ident, UL number and Date Code (YY/WW format) in this area as silkscreen on the bottom side.
13. For details of the impedances requirements, see the impedance notes below.
14. THE PCB VENDOR SHALL PROVIDE PROOF OF MEASUREMENT OF IMPEDANCE AND TEST COUPON

4 LAYER STACK UP DETAILS



IMPEDANCE CONTROL NOTES

The stackup and trace/gap widths above are designed to achieve 50-ohm impedance controlled traces on Layer 1 using "Grounded Co-Planar Waveguide" technology for the following trace width, and trace/copper gap ....

- Trace Width: 0.38mm traces on Layer 1 (Top Side).
- Trace/copper gap: 0.139mm

There shall be no deviation from this stack-up without the written permission of Analog Devices.