

ADF7030-1 Software Reference Manual

SCOPE

This manual provides a detailed description of how to control the [ADF7030-1](#) transceiver from the host microcontroller. It is intended as a resource for the firmware (FW) engineer developing host microcontroller firmware to communicate with the [ADF7030-1](#).

ABOUT THE ADF7030-1

The [ADF7030-1](#) is a low power, high performance, integrated radio transceiver supporting narrow-band and wideband operation in the <1 GHz industrial, scientific, and medical (ISM) bands. The [ADF7030-1](#) features an on-chip Arm® Cortex®-M0 processor that performs radio control and packet management.

FUNCTIONAL BLOCK DIAGRAM

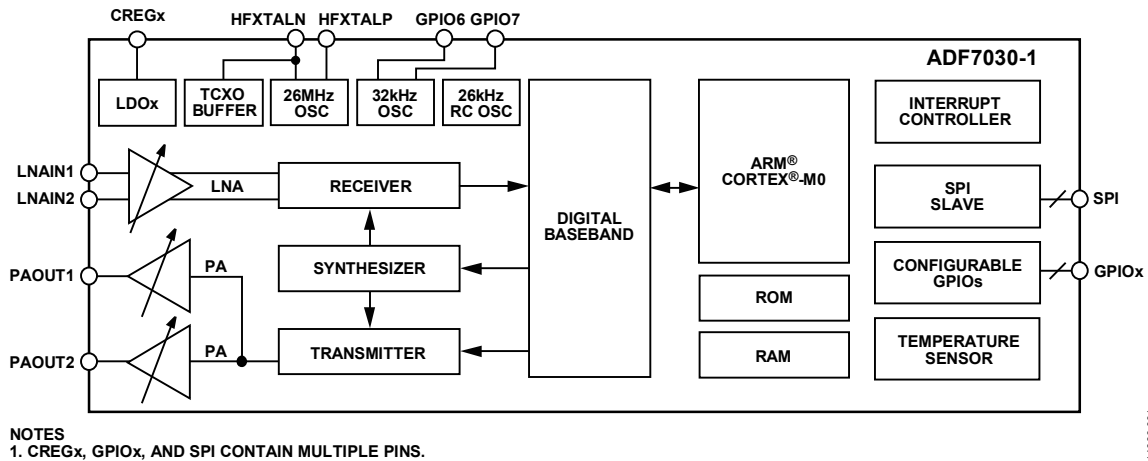


Figure 1. [ADF7030-1](#) Functional Block Diagram

146865-001

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REVISION HISTORY**6/2018—Rev. A to Rev. B**

Changed IEEE802.15.4g to IEEE802.15.4g-2012	Universal
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Added Sample Driver Section	7
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1/2017—Rev. 0 to Rev. A

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6/2016—Revision 0: Initial Version

INTRODUCTION

ADF7030-1 OPERATION

The ADF7030-1 is a very low power, high performance, highly integrated 2FSK/2GFSK/4FSK/4GFSK transceiver designed for operation in the 169.4 MHz to 169.6 MHz, 426 MHz to 470 MHz, and 863 MHz to 960 MHz frequency bands.

The ADF7030-1 supports the multirate frequency shift keying (MR-FSK) physical layer (PHY) 802.15.4g specified in IEEE 802.15.4g™-2012 standard with forward error correction (FEC), whitening, and interleaving at data rates of up to 150 kbps. The ADF7030-1 also supports a proprietary generic packet format. In addition, the ADF7030-1 supports a raw packet format that allows a host to perform packet parsing as data octets are received.

The ADF7030-1 is highly configurable. Begin by generating a configuration for the use case with the ADF7030-1 design center, which can be downloaded from the Analog Devices, Inc., website. Settings that can be altered at run time are described in this document.

In generic packet transmit (Tx) mode, the ADF7030-1 can be configured to add preamble, sync word, and cyclic redundancy check (CRC) to the payload data stored in the packet memory. The number of preamble bits and sync bits is programmable, and an optional length field can be added to allow packet length decoding at the receiver. In generic packet receive (Rx) mode, the ADF7030-1 can detect, and be configured to interrupt the host processor on, various packet related events (for example, preamble detected, sync word match, and valid CRC) and store the received payload to the packet memory. The CRC polynomial and length are fully programmable in generic packet mode.

Smart wake mode (SWM) allows the ADF7030-1 to wake up autonomously from sleep using the internal real-time clock (RTC) without intervention from the host processor. For systems requiring very accurate wake-up timing, an external 32 kHz oscillator can be used to drive the RTC. Alternatively, the internal resistor/capacitor (RC) oscillator can be used, which consumes less current in sleep. The host can trigger a wakeup from sleep using external signals. Contact Analog Devices for support on SWM.

The ADF7030-1 operates a radio state machine that presents a simple programming model to the host, comprising defined radio states that can be traversed by host commands to the radio. Following application of power to the radio, the ADF7030-1 autonomously enters the PHY_OFF state. The host must configure the ADF7030-1 with memory writes through the ADF7030-1 serial peripheral interface (SPI). After the host has configured the ADF7030-1, the host can then command the ADF7030-1 into other radio states using single-byte commands that trigger transitions. The host typically issues these commands over the SPI. However, the radio can also be configured to respond to an external interrupt as if it is a specified command.

ADF7030-1 MEMORY ARCHITECTURE

The ADF7030-1 contains 12 kB of random access memory (RAM), 4 kB of which is battery backed random access memory (BBRAM). The RAM starts at Address 0x2000 0000 within the memory map of the ARM Cortex-M0 microprocessor that is at the core of the ADF7030-1. The BBRAM stores the settings of the ADF7030-1 and this configuration is accessible by the host over the ADF7030-1 SPI. The BBRAM of the ADF7030-1 is partitioned into several regions. The ADF7030-1 stores radio settings such as channel frequency, data rate, and filter coefficients in the radio profile and lookup tables (LUTs) regions. The ADF7030-1 stores packet related settings such as packet format, payload length, and sync word in the generic packet region. The host writes packet data for transmission to the packet memory region, and the host reads received packet data from the packet memory region. The other regions within the ADF7030-1 memory are reserved for internal use, including space reserved for firmware modules that Analog Devices supplies to extend the functionality of the ADF7030-1. Several ADF7030-1 hardware registers are also accessible over the SPI to allow the host to control features such as controlling selected ADF7030-1 external interrupts. These registers are not shown in the memory map in Figure 2. Volatile RAM is reserved for potential firmware patches to enable additional functionality.

When powered up from cold (that is, battery applied), some default settings are initialized within the ADF7030-1 memory regions. However, these settings do not constitute a full configuration and, therefore, it is the responsibility of the host to initialize the ADF7030-1 settings to the desired values for the application.

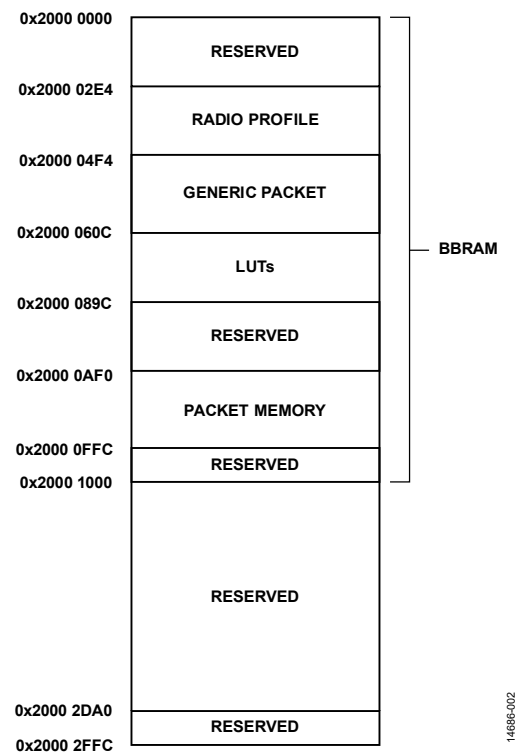


Figure 2. ADF7030-1 RAM Layout

DEVELOPMENT SUPPORT

DESIGN PACKAGE

The [ADF7030-1](#) design resource package is a complete documentation and resource package for the [ADF7030-1](#). It is recommended to download this package as a starting point for evaluation and development from the [ADF7030-1](#) product page. It contains manuals, application notes, hardware information, and firmware modules.

DOCUMENTATION

[ADF7030-1 Data Sheet](#)

The [ADF7030-1](#) data sheet contains the complete specifications and typical performance characteristics for the [ADF7030-1](#). Consult the data sheet in conjunction with this reference manual.

[ADF7030-1 Software Reference Manual \(UG-1002\)](#)

The [ADF7030-1 Software Reference Manual](#) is the detailed programming guide for the device. The [ADF7030-1 Hardware Reference Manual](#) provides a description of the [ADF7030-1](#) hardware features and application circuit requirements.

[ADF7030-1 Hardware Reference Manual \(UG-957\)](#)

The [ADF7030-1 Hardware Reference Manual](#) provides a description of the [ADF7030-1](#) radio functionality, hardware features, and application circuit requirements. It is intended as a resource for a hardware engineer designing a printed circuit board (PCB) that includes the [ADF7030-1](#).

EVALUATION KITS

Evaluation and development kits are available that include the [ADF7030-1](#) radio daughter boards. The [ADF7030-1 EZ-KIT*](#) is an evaluation and development system for the [ADF7030-1](#) high performance, sub-GHz, radio frequency (RF) transceiver, and includes four models. These kits are listed in Table 1.

Table 1. [ADF7030-1 EZ-KIT](#) Models

Model	Frequency (MHz)
ADF70301-915EZKIT	902 to 928
ADF70301-868EZKIT	863 to 876
ADF70301-433EZKIT	433 to 434
ADF70301-169EZKIT	169

A selection of individual daughter boards is also available covering various frequency bands and matching topologies.

EVALUATION SOFTWARE

The [ADF7030-1](#) design center can be used for configuring the [ADF7030-1](#), evaluating transmit and receive operation, and transmitting and receiving packets. This [ADF7030-1](#) design center allows the user to rapidly prototype different configurations with the [ADF7030-1](#) and simplifies the migration to host code development.

SAMPLE DRIVER

A device driver for the [ADF7030-1](#) is available on the [ADF7030-1](#) page on the Analog Devices website under Software & Systems Requirements. Examples are included for the [ADF7030-1 EZ-KIT](#) based evaluation platform.

ADF7030-1 STATE MACHINE

INTRODUCTION

The ADF7030-1 implements a state machine that the host controls via commands. The ADF7030-1 executes a transition from the current state to the next state in response to a command received from the host. These transitions are shown as solid lines in Figure 3. The ADF7030-1 also executes autonomous transitions, shown as dotted lines in Figure 3.

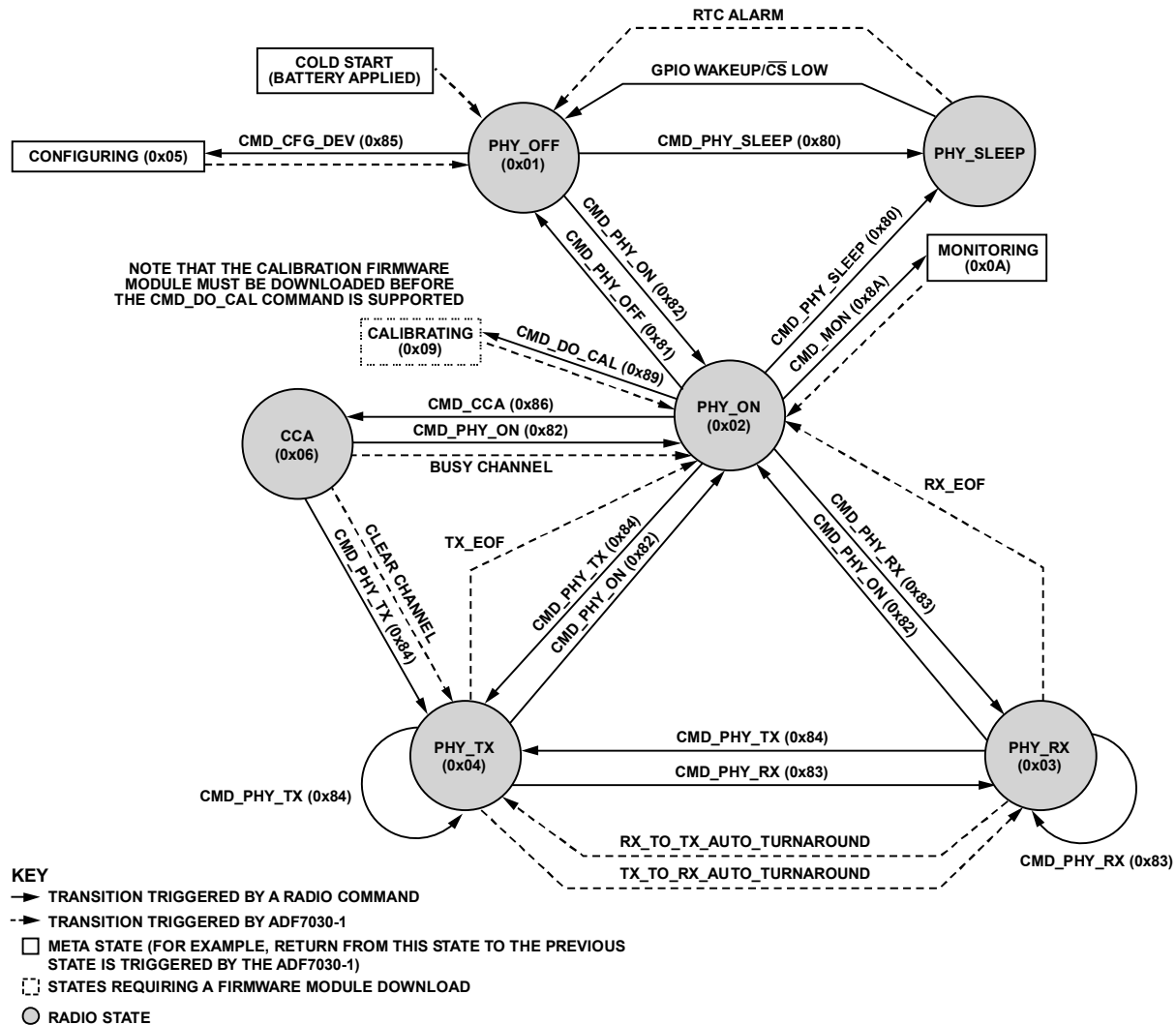


Figure 3. ADF7030-1 State Machine

ADF7030-1 STATES

PHY_OFF

The PHY_OFF state is the default state entered by the ADF7030-1 following a cold start, system reset, or when exiting from the PHY_SLEEP state. In the PHY_OFF state, the ADF7030-1 is running using its own internal oscillator clock. The ADF7030-1 transitions into the PHY_OFF state from the PHY_SLEEP state on a wake-up event (RTC alarm, GPIO2 and GPIO4 if configured as interrupt request (IRQ) inputs, or an SPI active low chip select (CS) low to high transition). In addition, the PHY_OFF state can be entered from the PHY_ON state and is entered autonomously from the configuring state. It is recommended that some of the ADF7030-1 settings be changed only when in the PHY_OFF state. The ADF7030-1 current in the PHY_OFF state is typically 1.9 mA and this increases to 3.7 mA if there has been a transition to PHY_ON and back to PHY_OFF.

PHY_SLEEP

The PHY_SLEEP state is the lowest current state of the ADF7030-1. In the PHY_SLEEP state, the ADF7030-1 memory regions are not accessible by the host (they are accessible by the host in all other states). The GPIOx configuration (direction and values) is retained while the ADF7030-1 is in the PHY_SLEEP state.

The host commands the ADF7030-1 to enter the PHY_SLEEP state from the PHY_OFF or PHY_ON state. When the host issues the CMD_PHY_SLEEP command in either of these two states, the ADF7030-1 turns off its internal regulators. The host enables ADF7030-1 BBRAM retention by setting the RETAIN_SRAM and enable bit in Register PROFILE_LPM_CFG0 before entering PHY_SLEEP. The host can also configure RTC related settings of the ADF7030-1 such that power is maintained to the ADF7030-1 internal RTC during the PHY_SLEEP state. The RTC can be configured to generate a periodic wake-up event to trigger an autonomous exit from the PHY_SLEEP state into the PHY_OFF state. The host must set the RETAIN_SRAM and enable fields before issuing a CMD_CFG_DEV command for the settings to take effect on entry into PHY_SLEEP.

To enable the retention of the ADF7030-1 BBRAM for a subsequent PHY_SLEEP transition, the host must set the RETAIN_SRAM and enable bit in Register PROFILE_LPM_CFG0 prior to issuing the CMD_CFG_DEV command.

Configuring

When in the PHY_OFF state, the host can update the ADF7030-1 configuration over the SPI by writing to memory regions and issuing the CMD_CFG_DEV command afterward. The ADF7030-1 state machine automatically returns from the configuring state to the PHY_OFF state when this configuration has completed. The CMD_CFG_DEV command must only be issued in the PHY_OFF state. The current in the configuring state is the same as the current in the PHY_OFF state prior to the host issuing the CMD_CFG_DEV command.

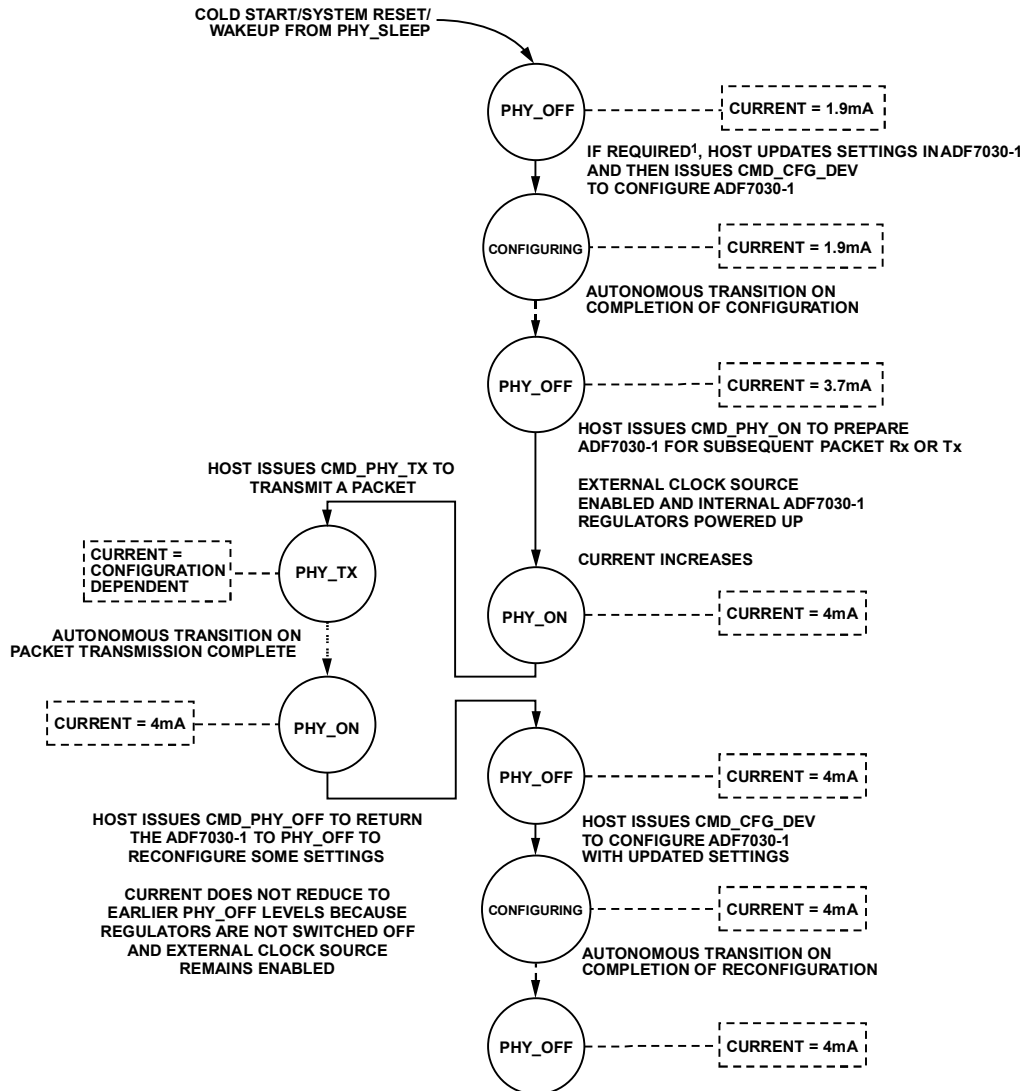
PHY_ON

In the PHY_ON state, the radio can quickly transition to PHY_RX to receive a packet or PHY_TX to transmit a packet. On its first transition from the PHY_OFF state to the PHY_ON state following a power cycle, system reset, or exit from PHY_SLEEP, the ADF7030-1 switches from using its internal oscillator to the external reference clock source, an external crystal (XTAL), or thermally compensated crystal oscillator (TCXO), as configured. The ADF7030-1 also powers up internal regulators in this first transition from PHY_OFF to PHY_ON.

The host must not issue a command to enter PHY_ON unless the ADF7030-1 has been configured using the CMD_CFG_DEV command since the last power cycle, system reset, or exit from PHY_SLEEP.

The host can change some ADF7030-1 settings in the PHY_ON state without the need to update the ADF7030-1 configuration via a CMD_CFG_DEV command. These settings include channel frequency and all packet related settings. The ADF7030-1 dynamically applies these settings to the hardware during the transition from PHY_ON to the PHY_CCA, PHY_TX, and PHY_RX states, without the need for an intervening CMD_CFG_DEV command from the host.

The ADF7030-1 current in the PHY_ON state is typically 3.7 mA.



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Figure 4. Example ADF7030-1 State Machine Configuration and Reconfiguration Indicating Current

PHY_TX

In the PHY_TX state, the ADF7030-1 transmits the packet data. The ADF7030-1 can be configured to autonomously transition from the PHY_TX state to the PHY_ON state once the ADF7030-1 has fully transmitted the packet. This autonomous transition is labeled TX_EOF in Figure 3. However, the ADF7030-1 can also be configured to autonomously transition from the PHY_TX state to the PHY_RX state (called Tx to Rx autoturnaround) after the ADF7030-1 has fully transmitted the packet. This autonomous transition is labeled TX_TO_RX_AUTO_TURNAROUND in Figure 3. The ADF7030-1 also supports transmission test modes including continuous carrier wave (CW) and pseudorandom binary sequence (PRBS) transmission. The host can command the ADF7030-1 to return to the PHY_ON state by issuing a CMD_PHY_ON command in the PHY_TX state. Any packet being transmitted at that time is aborted. The host can also command the ADF7030-1 to enter the PHY_RX state by issuing a CMD_PHY_RX command. Any packet being transmitted at that time is aborted. The ADF7030-1 current in the PHY_TX state depends on ADF7030-1 settings, such as transmission power and data rate. See the Transmitting and Receiving Packets section for more details on packet transmission.

PHY_RX

In the PHY_RX state, the ADF7030-1 receives packets. The ADF7030-1 can be configured to autonomously transition from the PHY_RX state to the PHY_ON state after the ADF7030-1 has received a packet (even if the received packet has an error such as CRC failure). This autonomous transition is labeled RX_EOF in Figure 3. The ADF7030-1 can also be configured to autonomously transition from the PHY_RX state to the PHY_TX state (called Rx to Tx autoturnaround) after the ADF7030-1 has received a packet without error. If the programmed CRC length, CRC_LEN in the GENERIC_PKT_FRAME_CFG0 register, is 0, a received packet is assumed to be valid. This autonomous transition is labeled RX_TO_TX_AUTO_TURNAROUND in Figure 3. The host can command a transition from the PHY_RX state to the PHY_ON state without having to wait for the ADF7030-1 to receive a packet by issuing a CMD_PHY_ON command. Any packet being received at that time is aborted. The ADF7030-1 current in the PHY_RX state depends on configuration settings such as data rate and packet format. See the Transmitting and Receiving Packets section for more details on packet reception.

Clear Channel Assessment (CCA)

In the CCA state, the ADF7030-1 continually measures the received signal strength indicator (RSSI) level and compares it against a configurable RSSI threshold, until the expiration of a configurable time interval. On the expiration of the time interval, the ADF7030-1 autonomously transitions from the CCA state to the PHY_TX state if the measured RSSI did not exceed the threshold at any instant during the time interval. If, however, the measured RSSI did exceed the threshold at any instant during the time interval, the ADF7030-1 returns to the PHY_ON state, when the time interval expires. These autonomous transitions are labeled clear channel and busy channel, respectively, in Figure 3. The result of the comparison is available for the host to interrogate. This functionality can be used by the host to support CCA functionality as specified in the IEEE 802.15.4g-2012 standard (Part 15.4) for MR-FSK. Note that packet reception is not possible during PHY_CCA.

Calibrating

The ADF7030-1 requires a system calibration that can be applied by downloading a firmware module supplied by Analog Devices. This is called the **OfflineCalibrations.cfg** module. The host must download this firmware module when the ADF7030-1 is in the PHY_OFF state. When the firmware is downloaded, the host can execute a system calibration by issuing the CMD_DO_CAL command from the PHY_ON state. The ADF7030-1 autonomously returns to the PHY_ON state after the system calibration is complete.

Following the autonomous return to PHY_ON, the host can read back specific values from the profile memory region that contains system settings optimized as a result of the system calibration. The host can write these values back to the profile memory region when the ADF7030-1 is in the PHY_OFF state, which reapplies the results of the previous system calibration without the need to issue a CMD_DO_CAL command.

Note that the **OfflineCalibrations.cfg** firmware module is not stored in battery backed up memory and, therefore, is not retained if the ADF7030-1 undergoes a power cycle, system reset, or exits the PHY_SLEEP state. In these instances, the host must reload the **OfflineCalibrations.cfg** firmware module in the PHY_OFF state before it can issue a CMD_DO_CAL command.

Monitoring

The host issues the CMD_MON command to the ADF7030-1 to measure and report the ADF7030-1 temperature in the PHY_ON state. The ADF7030-1 autonomously returns to the PHY_ON state on completion. The ADF7030-1 reports the temperature as a signed number in units of 0.0625°C.

STATE TRANSITION TIMING

Consult the ADF7030-1 data sheet for state transition timing information.

ADF7030-1 SPI

INTRODUCTION

The ADF7030-1 provides an SPI to facilitate configuration and control by a host. The host uses the SPI to read and write ADF7030-1 memory and registers, to issue commands, track the status of the state machine, and to wake up the ADF7030-1 from PHY_SLEEP. The ADF7030-1 operates as an SPI slave.

SPI PINS

The SPI connections between the host and ADF7030-1 are as shown in Table 2.

Table 2. Host Interface Connections

Generic SPI Signal Name	Description	ADF7030-1 Pin Name	Direction
SPI Chip Select Enable	Host brings this line low to select the SPI slave for SPI data exchange	CS	Host to ADF7030-1
SPI Clock	Host drives this signal to clock serial data in and out of the SPI slave	SCLK	Host to ADF7030-1
SPI Master Output, Slave Input (MOSI)	Serial data sent from the SPI master to the SPI slave	MOSI	Host to ADF7030-1
SPI Master Input, Slave Output (MISO)	Serial data sent from the SPI slave to the SPI master	MISO	ADF7030-1 to host

SPI Chip Select Enable

The host must connect its SPI slave enable signal to the $\overline{\text{CS}}$ input of the ADF7030-1. To initiate an SPI transaction, the host drives $\overline{\text{CS}}$ low before the first SCLK rising edge and drives it high again after the last SCLK falling edge. The ADF7030-1 ignores the SPI SCLK and MOSI signals while its $\overline{\text{CS}}$ input is high.

SPI SCLK

SCLK is the serial clock driven by the host to the ADF7030-1.

SPI MOSI and SPI MISO

MOSI is the data input line driven from the host to the ADF7030-1, and MISO is the data output from the ADF7030-1 to the host. MOSI and MISO are launched on the falling edge of SCLK and sampled on the rising edge of SCLK by the host and the ADF7030-1, respectively. MOSI carries the data from the host to the ADF7030-1. MISO carries the returning read data fields from the ADF7030-1 to the host during a read transaction. If a valid logic state on MISO is required at all times by the host, an external weak pull-up/pull-down resistor must be added on the PCB.

HOST INITIALIZATION OF ADF7030-1 SPI

On cold start system reset or wakeup from PHY_SLEEP, the host must wait until the ADF7030-1 SPI is ready for a SPI command transfer. The sequence the host must follow to issue the first SPI command is as follows (refer to the digital timing specifications in the ADF7030-1 data sheet for details of exact sequence):

1. The host brings $\overline{\text{CS}}$ low (if the ADF7030-1 is in PHY_SLEEP, this wakes up the device).
2. The host must monitor MISO and wait until it goes high. No SPI clock is needed for this to occur.
3. The host brings $\overline{\text{CS}}$ high. The SPI is now ready for an SPI command.

SPI TRANSACTIONS

The host is the master of the SPI and the following requirements must be met:

- When $\overline{\text{CS}}$ is brought low for an SPI transfer, a multiple of eight clock cycles must be generated by the host. Partial or fragmented transfers (for example, 33 clocks) are not supported.
- In every octet, the MSB (Bit 7) is transmitted or received first. This bit is followed by the next MSB (Bit 6), and so on (Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0).
- If the $\overline{\text{CS}}$ line is brought high at any time by the host, the [ADF7030-1](#) is ready to accept a new SPI transaction when $\overline{\text{CS}}$ is brought low again by the host.
- Data transfers consisting of multiple bytes can be achieved without having to deassert and reassert $\overline{\text{CS}}$ at any stage during the transfer (contingent on the first requirement of the clock cycles being in multiples of 8). This feature allows the host to design a SPI driver that does not require repeated configuration and restarting, as is typically necessary, making a host-based direct memory access (DMA) solution ideal.

SPI Transaction Timings

See the [ADF7030-1](#) data sheet for SPI interface timing specifications.

ADF7030-1 SPI COMMUNICATION

COMMAND BYTE

The host controls the ADF7030-1 over the SPI interface. The ADF7030-1 implements a simple protocol to which the host must conform. The first byte of MOSI data in an SPI transaction (defined as data transferred when CS is active low) is the command. The ADF7030-1 uses the CNM bit of the command to differentiate between a radio command and a memory command. Table 3 shows the format of the command.

Table 3. Command Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNM	Command dependent fields						

RADIO COMMANDS

The host controls the ADF7030-1 by issuing radio commands over the SPI.

A radio command triggers the ADF7030-1 to execute an immediate transition from the current state to a commanded state. The host also uses a radio command to configure the ADF7030-1 to execute a state machine transition in response to a signal on a configurable GPIOx pin. The host can also trigger an ADF7030-1 system reset by issuing a radio command.

In response to a radio command from a host, the ADF7030-1 sets a CMD_READY bit that indicates that the command has been received. When set, this bit also indicates that the host can issue another command (for example, to abort the current transition). Finally, when set, this bit indicates to the host that it can read a specific ADF7030-1 register that reflects the state of the ADF7030-1 state machine.

The ADF7030-1 makes the CMD_READY bit available over the SPI. The host can configure the ADF7030-1 to generate an interrupt when CMD_READY goes high.

Radio Commands to Trigger a State Machine Transition

The format of a radio command that triggers the ADF7030-1 to execute a transition between states is shown in Table 4. The host sets the desired destination state in Bits[4:0]. The host must guarantee that the transition between the current state and the requested state is supported as shown in Figure 3. If an unsupported transition is commanded, the ADF7030-1 remains in the current state.

Table 4. Radio Command Format for State Machine Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNM = 1	SPCNTRN = 0	Reserved = 0	Destination state (see Table 5)				

Table 5. State Machine Radio Commands

Command	Destination State	Description of ADF7030-1 Action
CMD_PHY_SLEEP	0x00	Performs a transition of the device into the PHY_SLEEP state
CMD_PHY_OFF	0x01	Performs a transition of the device into the PHY_OFF state
CMD_PHY_ON	0x02	Performs a transition of the device into the PHY_ON state
CMD_PHY_RX	0x03	Performs a transition of the device into the PHY_RX state to receive a packet
CMD_PHY_TX	0x04	Performs a transition of the device into the PHY_TX state to transmit a packet
CMD_CFG_DEV	0x05	Configures the ADF7030-1
CMD_CCA	0x06	Performs CCA
CMD_DO_CAL	0x09	Executes device calibration (requires the OffLineCalibrations.cfg FW module)
CMD_GPCLK	0x10	A nonreturnable state where a programmable clock is generated on the selectable GPIOx pin
CMD_MON	0x0A	Measures and reports the ADF7030-1 temperature
CMD_LFRC_CAL	0x0C	Performs low frequency RC (LFRC) oscillator calibration for the internal 26 kHz RC oscillator

Tracking State Machine Transitions

The ADF7030-1 provides several methods by which a host can track its state machine transitions.

Using the CMD_READY Event

The ADF7030-1 generates a CMD_READY event when it has started the transition to the commanded state. This event can be configured to generate an interrupt to the host (see the Clearing Interrupts section). This event also indicates that the host can read the MISC_FW register that contains the current state of the ADF7030-1 state machine. Additionally, this event indicates that the host can send another radio command to abort the current transition.

Using the SM_IDLE Event

The ADF7030-1 generates the SM_IDLE event to indicate when the ADF7030-1 has completed the commanded transition. This event can be configured to generate an interrupt to the host (see the Clearing Interrupts section). As an example of its use, if the current state of the ADF7030-1 is PHY_OFF and the host commands a transition to the PHY_ON state (command = 0x82), the ADF7030-1 generates the SM_IDLE event when the transition to PHY_ON has completed.

Autonomous Transitions

The ADF7030-1 executes some transitions autonomously. For example, when the ADF7030-1 is in the PHY_ON state and the host commands a transition to the PHY_TX state (command = 0x84), the ADF7030-1 does not generate the SM_IDLE event until the ADF7030-1 has completed the autonomous transition back to PHY_ON state after the packet transmission has completed. In this case, the SM_IDLE event indicates the ADF7030-1 has completed a chain of transitions initiated by a single radio command.

Using the ADF7030-1 Status over SPI

The ADF7030-1 also reports status via a status byte. The ADF7030-1 returns this byte on the SPI MISO pin in response to a no operation (NOP), 0xFF, on the SPI MOSI. The format of the status byte is shown in Table 6.

This status byte contains the CMD_READY in Bit 5. The status byte also contains the TRANSITION_STATUS field. This field reflects the phases of a transition of the ADF7030-1 state machine.

Table 6. ADF7030-1 Status Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	CMD_READY	Reserved	ERR	TRANSITION_STATUS		Reserved

Table 7. ADF7030-1 Status Byte Descriptions

Bit No.	Bit Name	Description
7	Reserved	Unused
6	Reserved	Unused
5	CMD_READY	0: the radio controller is not ready to receive a radio controller command 1: the radio controller is ready to receive a radio controller command
4	Reserved	Unused
3	ERR	Error code, indicating an error has occurred.
[2:1]	TRANSITION_STATUS	0: transition in progress 1: executing in a state 2: idle in a state
0	Reserved	Unused

Using the MISC_FW Register

The ADF7030-1 updates an internal register called MISC_FW that reflects the current state of the ADF7030-1 state machine. The encoding of the CURR_STATE field of the MISC_FW register of the ADF7030-1 matches that of the destination state field in Table 4. This register also contains the transition status field that is available in the SPI status byte. It is recommended that the host read the MISC_FW register only after the CMD_READY bit has gone high following a radio command.

The format of the MISC_FW register is shown in Table 8.

Table 8. MISC_FW Format

Bits[31:24]	Bits[23:14]	Bits[13:8]	Bits[7:2]	Bits[1:0]
ERR_CODE ¹	Reserved	CURR_STATE (see Table 87)	Reserved	TRANSITION_STATUS (see Table 6)

¹ ERR_CODE is the readback of the error code description.

Issuing a Radio Command over the SPI

In response to receiving a radio command from the host, the ADF7030-1 clears the CMD_READY bit. Clearing this bit indicates to the host that the ADF7030-1 is not yet ready to receive another radio command. While CMD_READY is low, the host must not write another radio command to the SPI slave.

The ADF7030-1 sets CMD_READY high to indicate to the host that it can send another radio command. Note that this does not indicate that the ADF7030-1 has completed the required actions associated with the radio command (for example, a state machine transition). Instead, it indicates that the radio command has been received and that the required actions associated with the radio command are in progress. The host can abort those actions by issuing another radio command any time after CMD_READY is high.

For example, having issued a CMD_PHY_TX command, the host, subsequent to seeing CMD_READY go high but before seeing the packet has finished transmitting, can issue CMD_PHY_ON to abort the transmission and return the ADF7030-1 state machine to the PHY_ON state.

RADIO COMMANDS FOR EXTERNAL HARDWARE TRIGGERED TRANSITIONS

The ADF7030-1 SPI protocol also supports radio commands that do not trigger a state machine transition. Using these configuration radio commands, the host can configure the ADF7030-1 to execute a transition in response to a signal from two of its GPIOx pins. This functionality is useful when it is desirable to configure the ADF7030-1 to execute a transition in response to periodically generated hardware events.

The host must only send these configuration radio commands when the ADF7030-1 is in the PHY_OFF or PHY_ON state. See Table 9 for the format of the command.

The ADF7030-1 supports two interrupt inputs, IRQ_IN0 and IRQ_IN1. The host can map these interrupt inputs onto any of the ADF7030-1 GPIOx pins (see the ADF7030-1 Interrupts section).

To use the interrupt inputs, the host first configures which transition the ADF7030-1 must execute if a rising signal is applied to IRQ_IN0 or IRQ_IN1 by writing a byte to the SM_CONFIG_GPIO_CMD_0 register or the SM_CONFIG_GPIO_CMD_1 register, respectively. The byte value written must be the same 8-bit radio command that generates the desired transition if it is sent over the SPI. Next, the host sends the radio command to enable the IRQ_IN0 interrupt or the IRQ_IN1 interrupt (see Table 9). The ADF7030-1 then executes the preconfigured radio command whenever a rising edge appears on the general-purpose input/output (GPIO) configured for IRQ_IN0 or IRQ_IN1.

Table 9. Configuration Radio Command Structure

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNM	SPCNTRN	Configuration command identifier					
1	1	See Table 10					

Table 10. Configuration Radio Command Identifier

Command	Configuration Command Identifier	Description of ADF7030-1 Action
CMD_IRQ1_DIS_IRQ0_DIS	0x0C	Disable hardware triggered transition
CMD_IRQ1_DIS_IRQ0_EN	0x0D	Disable IRQ_IN1 and enable IRQ_IN0 for triggering preloaded radio commands
CMD_IRQ1_EN_IRQ0_DIS	0x0E	Enable IRQ_IN1 and disable IRQ_IN0 for triggering preloaded radio commands
CMD_IRQ1_EN_IRQ0_EN ¹	0x0F	Enable IRQ_IN1 and IRQ_IN0 for triggering preloaded radio commands

¹ In addition to (and subsequent to) the Radio Command 0x8F enabling both interrupts, the host must write a value of 0x0808 to the 16-bit data word at Address 0x40003818.

Example of GPIO Triggered Transitions

For the host to trigger a PHY_ON to PHY_TX transition using a low to high transition on a GPIOx pin and a PHY_ON to PHY_OFF state transition using a low to high transition on a separate GPIOx pin, follow these steps:

1. Configure the selected GPIOs as interrupt inputs, IRQ_IN0 and IRQ_IN1 (see the ADF7030-1 Interrupts section).
2. Preload the commands.
 - a. The host writes the command value for CMD_PHY_TX (0x84) into the 8-bit location at SM_CONFIG_GPIO_CMD_0.
 - b. The host writes the command value for CMD_PHY_OFF (0x81) into the 8-bit location at SM_CONFIG_GPIO_CMD_1.
3. Enable the interrupt inputs.
The host enables the ADF7030-1 to execute the preloaded command in response to a rising edge on the IRQ_IN0 or IRQ_IN1 input, respectively, by sending the CMD_IRQ1_EN_IRQ0_EN (0xCF) configuration radio command to the ADF7030-1 over the SPI.

As a result, the ADF7030-1 is configured so that a rising edge on the ADF7030-1 GPIOx pin configured as IRQ_IN0 is equivalent to sending a CMD_PHY_TX command over the SPI to the ADF7030-1.

Similarly, the ADF7030-1 is configured so that a rising edge on a GPIOx pin configured as IRQ_IN1 is equivalent to sending a CMD_PHY_OFF command over the SPI to the ADF7030-1.

The host can track the transition triggered with this method in the same manner as if the radio command was sent over the SPI.

RADIO COMMAND FOR A SYSTEM RESET

The host can reset the ADF7030-1 over the SPI using the following sequence:

1. Set Bit 15 and Bit 22 of the CRMGT_PROC_CLK_EN register to 1. Read the register and then write the new value using a 32-bit SPI write (see the Accessing the ADF7030-1 Memory section).
2. Write 0x27 to the SW_KEY bit of the PMU_KEY register using a 32-bit SPI write.
3. Immediately write 0x1 to the HFRC_PD_N bit of the PMU_CLOCKS register using a 32-bit SPI write.
4. Issue the 0xC7 radio reset command to perform a full system reset of the radio.

ACCESSING THE ADF7030-1 MEMORY

INTRODUCTION

The ADF7030-1 SPI supports a flexible memory access protocol that allows the host to access the ADF7030-1 memory efficiently. The protocol supports auto-incrementing addressing for reading or writing blocks of data, base plus offset addressing using three dedicated base address pointers in the ADF7030-1, and individual byte and 4-byte word transfers. See the Host to ADF7030-1 Memory Access Modes section for information about the order of the SPI MISO and SPI MOSI data for each memory protocol. The host is free to choose the protocol that best suits the design of the host SPI.

The host uses the SPI memory access protocols to read and write the memory regions of the ADF7030-1. The format of the SPI transaction starts with a command word with the CNM bit = 0.

The host does not need to monitor the CMD_READY bit before it can read or write ADF7030-1 memory.

All ADF7030-1 RAM can be accessed using byte wide accesses. However, some ADF7030-1 registers must only be accessed using a 32-bit data protocol. This restriction is detailed where relevant.

SUMMARY AND RECOMMENDATIONS

There are eight different memory access modes (see Table 11).

Table 11. Access Modes

Address Mode	Recommended for Accessing
Memory Write/Read, Block, No Pointer, Long Address	One block of 4-byte words written or read once
Memory Write/Read, Block, Pointer Base with Offset Address, Short Address	Different subblocks of bytes written or read often within a larger block of data
Memory Write/Read, Block, Pointer, Long Address	One block of 4-byte words written or read often
Memory Write/Read, Block, Pointer, Short Address	One block of bytes written or read often
Memory Write/Read, Random, No Pointer, Long Address	One 4-byte word written or read once
Memory Write/Read, Random, Pointer Base with Offset Supplied, Short Address	Different single bytes written or read from within a block
Memory Write/Read, Random, Pointer, Long Address	One 4-byte word written or read often
Memory Write/Read, Random, Pointer, Short Address	One byte written or read often

FORMAT OF MEMORY ACCESS COMMAND

The format of the command byte for memory accesses command is shown in Table 12. See Table 13 for the bit descriptions.

Table 12. Memory Access Command

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNM = 0	RNW	BNR	ANP	LNS	MPTR		

Table 13. Memory Access Command Bit Descriptions

Bit No.	Bit Name	Description
6	RNW	Read, not write. 0: writes for the duration of the current \overline{CS} active low time. 1: reads for the duration of the current \overline{CS} active low time.
5	BNR	Block (burst), not random, auto-incrementing address indicator for memory transfers. 0: execute random memory accesses whose address has no connection with any foregoing transfer during the same \overline{CS} low time. 1: block (burst) memory accesses, whereby each access has its address auto-incremented from the immediately foregoing access during the same \overline{CS} low time.
4	ANP	Address, not pointer, address source indicator for memory transfers. 0: no address information is supplied by the host for either long or short format memory transfers. Exclusively pointer-based addresses are used instead. 1: host supplies a full address for long format memory transfers and a pointer address offset for short format memory transfers.
3	LNS	Long, not short, memory transfer width format. 0: issue a short format, pointer-based, optionally offset, byte wide, byte aligned memory transfer. 1: issue a long format, 32-bit, word aligned, host specified memory transfer.

Bit No.	Bit Name	Description
[2:0]	MPNTR	Base address selection for pointer-based memory accesses. 000: used to set up Pointer 0, Pointer 1, and Pointer 2. 001: reserved. 010: reserved. 011: reserved. 100: reserved. 101: use the contents of Pointer 0 as the base address for pointer-based memory transfers. 110: use the contents of Pointer 1 as the base address for pointer-based memory transfers. 111: use the contents of Pointer 2 as the base address for pointer-based memory transfers.

CONFIGURING THE POINTERS FOR POINTER BASED ACCESSES

The host can configure each of the three [ADF7030-1](#) pointers with a 32-bit address for pointer-based addressing. The SPI command used to write to the pointers is 0x28: memory access (CNM = 0), write (RNW = 0), block (BNR = 1), pointer (ANP = 0), long format (LNS = 1), access pointers themselves (MPNTR = 000). See the Memory, Block, Pointer, Long Address section for more information.

CONFIGURING THE ADF7030-1

The ADF7030-1 transceiver can be configured for different frequency bands, data rates, frequency deviations, and packet formats. From a user perspective, configuring the ADF7030-1 entails writing register settings to the BBRAM section of the radio memory over the SPI. The layout of the radio memory is described in the ADF7030-1 Memory Architecture section. See Figure 2 for an overview of the memory layout.

From a user perspective, the ADF7030-1 has the following three sections in memory used for configuring the radio:

- The radio profile area, PROFILE, stores the radio RF settings. This area includes the channel frequency, CCA settings, low power mode configuration, and GPIO configuration.
- The packet area, GENERIC_PACKET, stores packet configuration settings for both the generic packet format and IEEE 802.15.4g-2012 packet format. This area includes the packet length, payload location, sync word or PHY header (PHR) length, and value and CRC/frame check sequence (FCS) configurations.
- Various lookup tables (LUTs) are stored in memory. These LUTs are used for configuring internal radio blocks and running and storing the results from calibrations.

As shown in the ADF7030-1 register map, the contents of the lookup tables and many of the fields in the profile and generic packet sections are labeled as generated. These fields are generated by the ADF7030-1 design center graphical user interface (GUI) based on the RF and packet settings of the user. This ADF7030-1 design center is part of the EZ-KIT® design suite, a set of tools for configuring and evaluating Analog Devices low power integrated transceiver products. The ADF7030-1 design center contains a **Radio Configuration** tab that allows a user to enter their desired RF and packet settings. The ADF7030-1 design center generates a corresponding configuration (CFG) file for these settings, containing all required radio settings, including the appropriate LUTs, that can then be written to the device by the user.

The first step in using the ADF7030-1, called the initial configuration, is applying the settings generated by the ADF7030-1 design center to the device. After this configuration step, a user can optionally choose to modify some settings while the device is running.

INITIAL CONFIGURATION

The following steps are required to set up the ADF7030-1 upon a cold startup:

1. Generate the user settings in the ADF7030-1 design center.
Enter the desired RF and packet settings in the **Radio Configuration** tab of the ADF7030-1 design center. This produces an ADF7030-1 configuration file to write to the radio. This file contains memory radio and packet configuration and the appropriate LUTs. See the ADF7030-1 Configuration File Format section for a detailed explanation of the configuration file format.
2. Write/download the user settings to the ADF7030-1.
The contents of the ADF7030-1 configuration file are written to the ADF7030-1 in PHY_OFF over the SPI. See the Host Initialization of ADF7030-1 SPI section for instructions on issuing a SPI command after a cold start or wakeup from sleep. See the Applying the ADF7030-1 Configuration section for a detailed explanation of how to interpret the configuration file and write it to the radio.
3. Apply the user settings.
The host microcontroller sends a CMD_CFG_DEV command. The radio returns to PHY_OFF. See the Configuring section for more information.

MODIFYING CONFIGURATION AT RUN TIME

Some radio and packet settings can be modified after the initial configuration step.

The ADF7030-1 settings can be subdivided into two categories, generated settings and run-time settings.

Generated Settings

These settings cannot be calculated by the user. They are generated by the ADF7030-1 design center and must not be overwritten by the user. Change these values only when a new, full configuration file is applied to the device. These private fields can be single or multiple bit fields in a register, marked as generated in the register map, or a full 32-bit register. Examples of a fully generated register include the PROFILE_OCL_CFG0 register.

Run-Time Settings

Run-time settings can be changed after the initial configuration by the user.

These fields are documented and public. They include fields from the radio profile, such as channel frequency, which can be changed in PHY_ON, for example, between an Rx and a Tx transfer. Another example is the power amplifier (PA) power and PA selection.

All packet configuration settings can be changed in PHY_OFF and PHY_ON, including, for example, the sync word and the payload length.

The interrupt source and pin output configuration can be reconfigured in PHY_OFF and PHY_ON, by changing, for example, the IRQ mask for IRQ_OUT0 to enable an interrupt on the preamble found interrupt.

GPIO functionality can be altered by the user at run time, by enabling, for example, the transmit or receive clock, SPORT_TRXCLK, on a selected pin. A CMD_CFG_DEV command is required for these changes to take effect.

The RTC period can also be changed, requiring a CMD_CFG_DEV command.

APPLYING THE ADF7030-1 CONFIGURATION FILE

An ADF7030-1 configuration file is a standardized file format for representing memory writes to the ADF7030-1. The ADF7030-1 configuration file format is used to store and apply radio settings, packet settings, lookup tables, and packet payload data generated by the ADF7030-1 design center to the radio. Firmware modules, such as the OfflineCalibration.cfg firmware module, are also supplied as configuration files.

ADF7030-1 CONFIGURATION FILE FORMAT

An ADF7030-1 configuration file is an ASCII text file. At the top of the file, a C99 ISO/IEC 9899:1999 standard compliant multilevel comment describes the content of the file and provides a version or time stamp.

There can be one or more blocks in an ADF7030-1 configuration file. A block represents a single SPI transaction and is formatted as a sequence of bytes separated by commas, that is, integers between 0 and 255, written in two-digit wide hexadecimal notation, for example, 0x2E. A block may be preceded by an additional C style comment. Each block starts with a framing header of three bytes, which contains the length of the block, including the length of the frame itself. The length header byte order is MSB first. For example, a block length of 300 bytes starts with a sequence of 0x00, 0x01, 0x2C, where 0x00012C is 300 in hexadecimal.

Table 14. ADF7030-1 Configuration File Block Format

Length Header	SPI Command Sequence
Three Bytes, MSB First	Sequence of Bytes

Table 15. Example of an ADF7030-1 Configuration File Block Format, Showing a Block Write to Address 0x2000060C

Length Header	SPI Commands		
Three Bytes Indicating a 16-Byte block	Block Write	Starting Address	8 Bytes of Data
0x00, 0x00, 0x0F	0x38	0x20, 0x00, 0x06, 0x0C	0xB1, 0xB2, 0xB3, 0xB4, 0xB5, 0xB6, 0xB7, 0xB8

The following is an example of a configuration file, where 0xL0, 0xL1, and 0xL2 are the length bytes in the block header of each block and 0xB1 to 0xBn are the data bytes to be written to the radio memory.

```
/*
*****
** use_case4.cfg source file generated on June 26, 2016 at 20:04:02
**
** Copyright (C) 2015-2016 Analog Devices Inc., All Rights Reserved.
**
** This file was generated automatically based upon parameters passed to the
** Calculator Library.
**
** For descriptions of each parameter, please refer to Calculator Library Help.
**
** CHANNEL_FREQUENCY                      915000000
** DATA_RATE                             12500.00
** FREQUENCY_DEVIATION                    50000.00
<TRUNCATED>
** TEST_MODES0_TX_TEST                    0
**
*/

/* Write to profile memory at 0x20002E4 with word access*/
0xL0, 0xL1, 0xL2, 0x38, 0x20, 0x00, 0x02, 0xE4,
0xB1, 0xB1, 0xB1, 0xB1, 0xB1, 0xB1, 0xB1, 0xB1
...
```

0xBn-3, 0xBn-2, 0xBn-1, 0xBn

The contents of the configuration file can be easily stored in a C array to assist in writing host microcontroller code.

```
const uint8_t Radio_Memory_Configuration[ ] = {  
#include "Settings_ADF7030-1.cfg"  
};
```

ADF7030-1 CALIBRATION

To ensure that the [ADF7030-1](#) radio performance meets the data sheet specifications, it is necessary to perform a calibration of the [ADF7030-1](#). The Analog Devices supplied firmware module, **OffLineCalibrations.cfg**, is required for calibration.

Calibration data is maintained in PHY_SLEEP if BBRAM retention is enabled (RETAIN_SRAM and enable bits in the PROFILE_LPM_CFG0 register are set to 1). If the BBRAM is not retained, the host must reload the calibration data to the [ADF7030-1](#) (see Figure 25).

CALIBRATION GUIDELINES

The [ADF7030-1](#) calibration is typically a one-time calibration that can be run as part of a factory calibration routine.

Refer to the [ADF7030-1](#) data sheet for further guidelines.

HOW TO RUN THE RADIO CALIBRATION

The following steps are required to perform a calibration of the [ADF7030-1](#) (see Figure 23):

1. Apply power to the [ADF7030-1](#) and allow it to transition to PHY_OFF.
2. With the [ADF7030-1](#) in the PHY_OFF state, apply the configuration file generated by the [ADF7030-1](#) design center for the desired use case, as described in the Applying the ADF7030-1 Configuration File section.
3. While still in the PHY_OFF state, apply the **OffLineCalibrations.cfg** firmware module.
4. Write the CAL_ENABLE key (0x20002971) to the SM_DATA_CALIBRATION register to enable the calibration.
5. Issue the CMD_CFG_DEV configuration command.
6. When the radio returns to the PHY_OFF state from the configuring state, issue the CMD_PHY_ON command to place the [ADF7030-1](#) in the PHY_ON state.
7. In the PHY_ON state, issue the CMD_DO_CAL command. The calibration typically takes 630 ms if all calibrations are enabled.
8. On completion of the calibration, the radio autonomously returns to the PHY_ON state and the CAL_SUCCESS bit in the PROFILE_RADIO_CAL_CFG1 register is set to 1.
9. Write the CAL_DISABLE key (0x20002A21) to SM_DATA_CALIBRATION.

The calibration results registers, as shown in Table 16, can be read back at this point and stored to facilitate a reload of the calibration settings to these same registers following a subsequent cold start, system reset, or wake from PHY_SLEEP without BBRAM retention.

The **OffLineCalibrations.cfg** firmware module is not retained if the [ADF7030-1](#) is put into the PHY_SLEEP state, even if BBRAM is retained. To prevent the radio from entering an undefined state during a calibration when the calibration firmware module is no longer present in memory, always disable the calibration by writing the CAL_DISABLE key to SM_DATA_CALIBRATION after a calibration has been performed.

The calibration results are stored in the registers listed in Table 16.

Table 16. Calibration Result Registers

Address	Register
0x200003C8	PROFILE_RADIO_CAL_RESULTS0
0x200003CC	PROFILE_RADIO_CAL_RESULTS1
0x200003D0	PROFILE_RADIO_CAL_RESULTS2
0x200003DC	PROFILE_RADIO_CAL_RESULTS5
0x200003E0	PROFILE_RADIO_CAL_RESULTS6
0x200003E4	PROFILE_RADIO_CAL_RESULTS7
0x200003E8	PROFILE_RADIO_CAL_RESULTS8
0x20000844	VCO_CAL_RESULTS_DATA0
0x20000848	VCO_CAL_RESULTS_DATA1
0x2000084C	VCO_CAL_RESULTS_DATA2
0x20000850	VCO_CAL_RESULTS_DATA3
0x20000854	VCO_CAL_RESULTS_DATA4
0x20000858	VCO_CAL_RESULTS_DATA5
0x2000085C	VCO_CAL_RESULTS_DATA6
0x20000860	VCO_CAL_RESULTS_DATA7

RESTORING SAVED CALIBRATION RESULTS TO THE ADF7030-1

Following a cold start, system reset, or wakeup from PHY_SLEEP without retained BBRAM, the calibration settings in the ADF7030-1 are lost. However, if the host has saved the results of the previous calibration, these results can be reloaded to the ADF7030-1. Saving the results avoids the necessity of having to rerun calibration, notwithstanding the fact that another calibration may be required because of a time lapse or temperature change.

To reload the results of the last calibration executed, the host processor must follow this sequence:

1. Command the ADF7030-1 into the PHY_OFF state if it is not already in that state.
2. Load the configuration settings into the ADF7030-1 (profile, generic packet, LUTs, packet memory).
3. Write the saved calibration results into the calibration results registers shown in Table 16 to the ADF7030-1.
4. Issue a CMD_CFG_DEV command.

The previous calibration settings are restored at this point.

TEMPERATURE SENSOR

The [ADF7030-1](#) contains a temperature sensor that returns the temperature as a 12-bit signed value in units of 0.0625°C in the TEMP_OUTPUT bits of the PROFILE_MONITOR1 register.

This [ADF7030-1](#) temperature sensor is not factory calibrated.

EXAMPLE CONVERSION

To read the temperature, the host must enter the monitoring state. After the TEMP_OUTPUT bits in the PROFILE_MONITOR1 register are written to by the [ADF7030-1](#), the state machine returns to the PHY_ON state.

$\text{PROFILE_MONITOR1_TEMP_OUTPUT} = 0x1E8$

Obtain the twos complement of TEMP_OUTPUT.

If $\text{TEMP_OUTPUT} > 2^{11}$, $\text{TEMP_OUTPUT} = \text{TEMP_OUTPUT} - 2^{12}$

Then multiply by 0.0625 to convert the unit to degrees Celsius.

$\text{Temperature } (^{\circ}\text{C}) = 488 \times 0.0625 = 30.5^{\circ}\text{C}$

TRANSMITTING AND RECEIVING PACKETS

OVERVIEW

The host programs the ADF7030-1 to transmit and receive variable or fixed length packets. In preparation for transmitting a packet, the host writes payload data into the ADF7030-1 Tx payload buffer and configures programmable fields in the generic packet memory region. The ADF7030-1 transmits a packet in response to a CMD_PHY_TX command.

In preparation for receiving a packet, the host configures programmable fields in the generic packet memory region and issues a CMD_PHY_RX command to the ADF7030-1. The ADF7030-1 then enters the receive state, PHY_RX. If a preamble is detected, the preamble interrupt is set. If the preamble then stops being received, the preamble gone interrupt is set. If subsequently the sync word specified in the packet configuration is detected, the ADF7030-1 proceeds to receive the payload and saves the payload of the packet in the Rx payload buffer.

As a packet is received or transmitted, the ADF7030-1 generates events that can be configured to cause external interrupts on the selected external GPIOx pins.

PACKET MEMORY

The ADF7030-1 packet memory is reserved for Rx and Tx payload buffers. The host configures a Tx payload buffer and an Rx payload buffer within the packet memory.

The host can overlap the Rx and Tx payload buffers or can configure two nonoverlapping payload buffers. The start locations of the Rx and Tx payload buffers are set via the PTR_RX_BASE and PTR_TX_BASE bits, respectively, in the GENERIC_PKT_BUFF_CFG0 register. By default, these fields both point to the start of the packet memory. The sizes of the Rx and Tx payload buffers are set via the RX_SIZE and TX_SIZE bits, respectively, in the GENERIC_PKT_BUFF_CFG1 register. By default, these bits are both 256 bytes. The host is responsible for ensuring that the Rx and Tx payload buffers do not extend outside the ADF7030-1 packet memory.

The maximum size of the Tx payload buffer is 511 bytes. The maximum size of the Rx payload buffer is 511 bytes. See the Rolling Buffers Mode section for payloads greater than 511 bytes.

Note that Analog Devices reserves the right to use the packet memory for future functionality upgrades. Contact Analog Devices to use space other than packet memory for the Rx and Tx payload buffers.

PACKET FORMATS

The ADF7030-1 supports two packet formats: generic and IEEE 802.15.4g-2012. The host selects the packet format used for Rx and Tx via the TYPE_FRAME0 bit in the PROFILE_PACKET_CFG register. The Generic Packet Format section and the IEEE 802.15.4g-2012 Packet Format section describe the supported packet formats.

GENERIC PACKET FORMAT

The generic packet format for Tx and Rx is shown in Figure 5 and Figure 6, respectively.

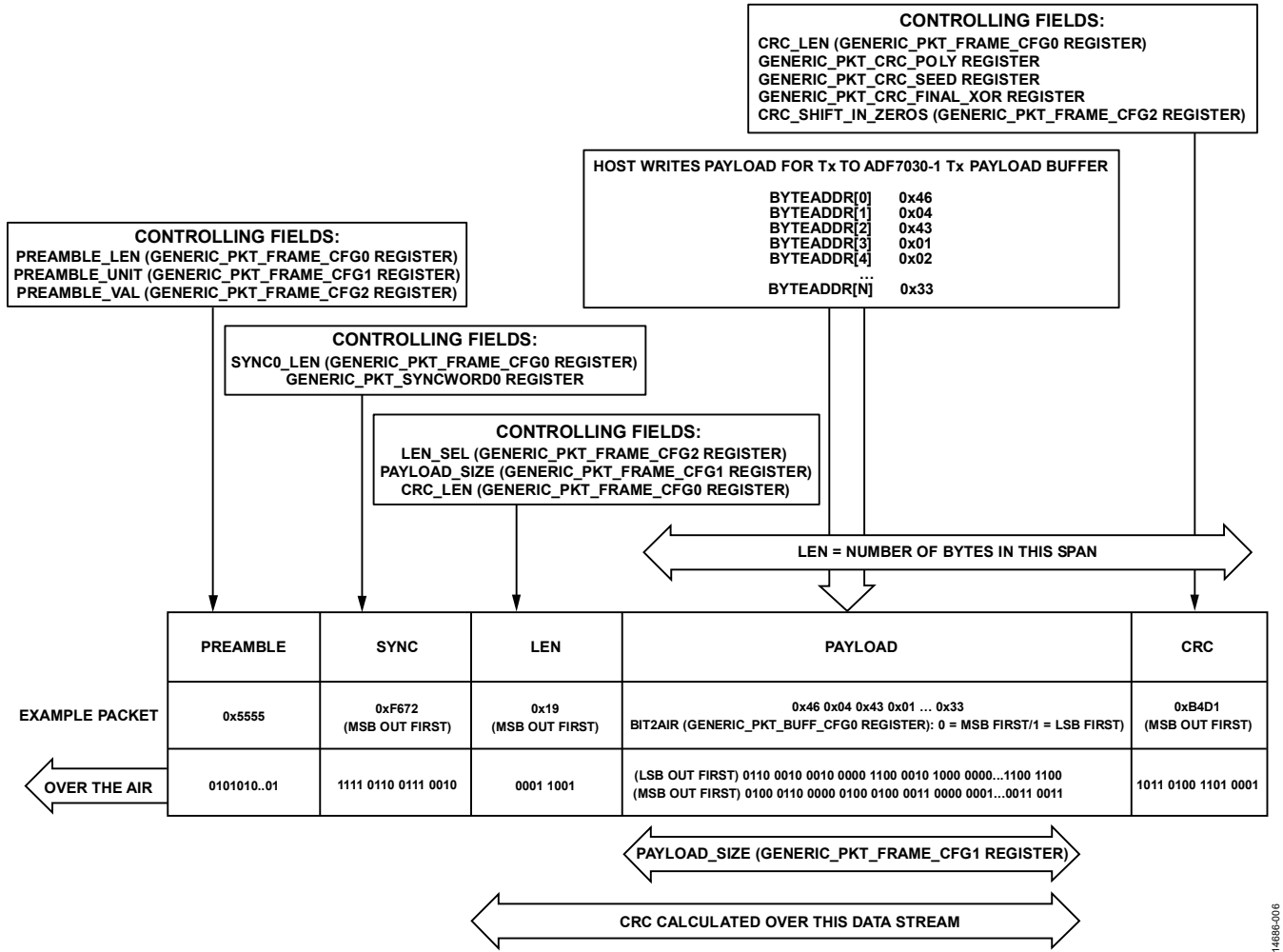


Figure 5. Generic Packet Structure for Tx

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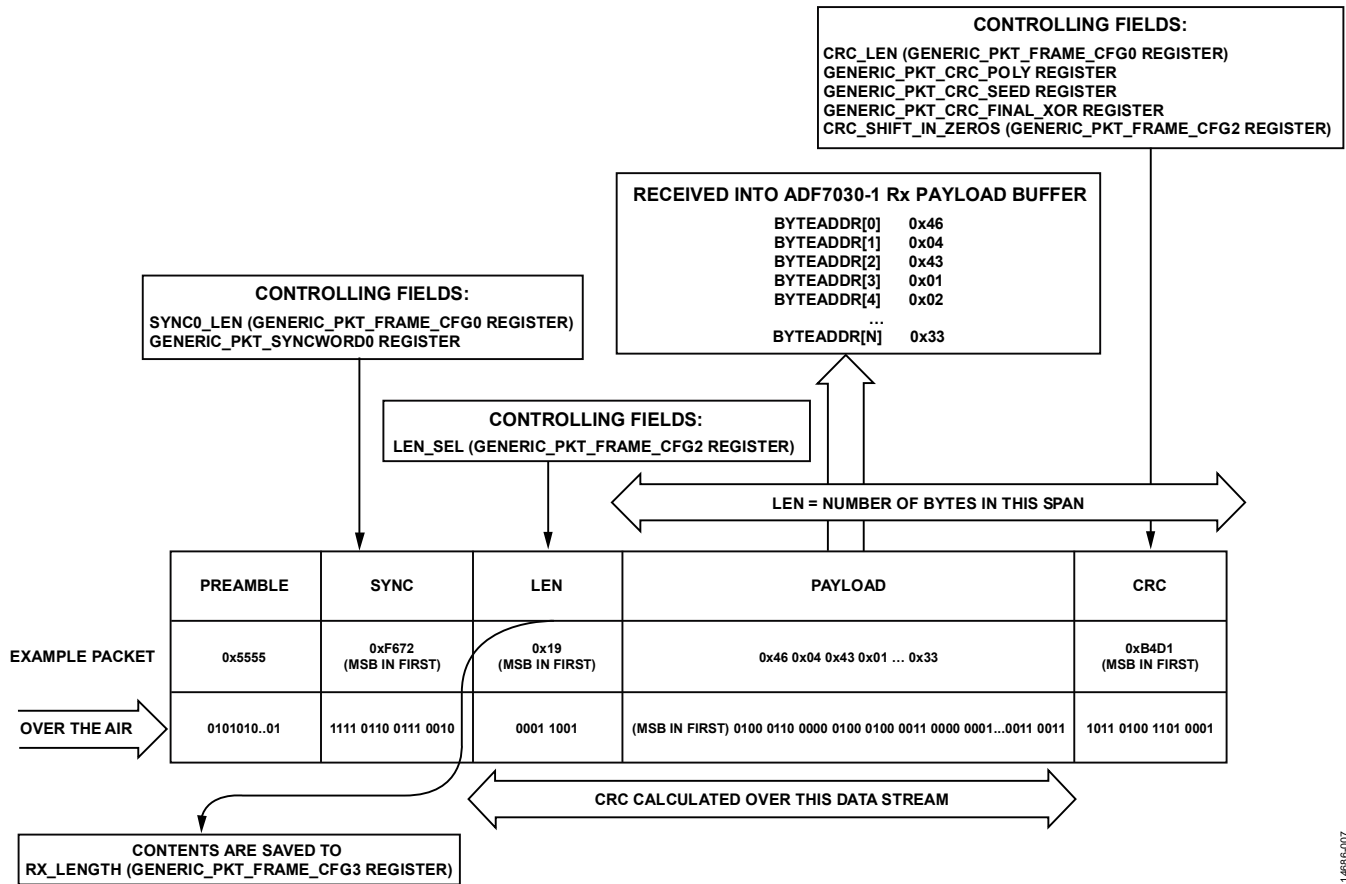


Figure 6. Generic Packet Structure for Rx

Generic Packet Tx

The following sections describe the bits used by the ADF7030-1 in transmitting a generic packet.

Preamble

The number of preamble bits transmitted is controlled by the PREAMBLE_UNIT bit in the GENERIC_PKT_FRAME_CFG1 register and the PREAMBLE_LEN bits in the GENERIC_PKT_FRAME_CFG0 register.

The preamble pattern transmitted is 0x55 by default. However, the host can program an alternative pattern for preamble transmission via the PREAMBLE_VAL bits in the GENERIC_PKT_FRAME_CFG2 register.

The ADF7030-1 generates the preamble detect event when the first bit of preamble is being transmitted. The ADF7030-1 generates the preamble gone event when the last bit of preamble has been transmitted.

Sync

The host specifies the number of bits of the sync word in a transmitted packet by the SYNC0_LEN bits in the GENERIC_PKT_FRAME_CFG0 register. Note that if this is less than 32, the LSBs of the GENERIC_PKT_SYNCWORD0 register are used to create the sync word. The sync word is transmitted over the air with the higher bits transmitted first.

The following restrictions apply to the sync word and preamble for a generic packet Tx:

- The value of the SYNC0_LEN bits in the GENERIC_PKT_FRAME_CFG0 register must be between 8 and 32, inclusive.
- $\text{SYNC0_LEN} + (\text{PREAMBLE_LEN} \times 2)$ must be at least 32.
- The ADF7030-1 generates the sync word detect event when the last bit of sync has been transmitted.